SYSTEM AND METHOD FOR REDUCING SHORTING IN MEMORY CELLS

Background of the Invention

Field of the Invention

[0001] The present invention relates to magnetic random access memory (MRAM) devices. More specifically, the present invention relates to reducing electrical shorting in the memory cells of an MRAM device.

Description of the Related Art

[0002] Magnetic random access memory (MRAM) is a well-known form of memory. In an MRAM device, digital bits of information can be stored as alternative directions of magnetization in a magnetic storage element or cell. The storage elements may be simple structures, such as thin ferromagnetic films, or more complex layered magnetic thin-film structures, such as tunneling magnetoresistance (TMR) or giant magnetoresistance (GMR) elements.

[0003] An exemplary TMR memory cell comprises two magnetic layers separated by a barrier layer. One magnetic layer, referred to as the "pinned" layer, has a fixed magnetization direction, whereas the magnetization direction of the other magnetic layer, referred to as the "sense" layer, can be reversed by applying a magnetic field that is not strong enough to affect the magnetization direction of the pinned layer.

[0004] A TMR memory cell can operate by allowing a quantum mechanical tunneling of electrons from one magnetic layer to the other through the barrier layer of the cell. The passage of electrons through the barrier layer depends upon the magnetization direction of the sense layer relative to that of the pinned layer. Electrons pass more freely when the magnetic directions of the layers are aligned and less freely when the magnetic directions of the layers are not aligned. Therefore, the state of a memory cell can be determined by observing the degree of electron tunneling through the barrier layer. GMR memory cells operate similarly by sensing current flow or resistance through aligned or anti-aligned magnetic layers, rather than by employing a tunneling dielectric.

[0005] A TMR memory cell cannot function properly unless the sense layer and the pinned layer of the cell are electrically isolated from one another. If a short circuit occurs between these two layers, then there will be no tunneling of electrons through the barrier layer.

[0006] A plurality of magnetic memory cells can be organized into an array having any of a wide variety of configurations. One exemplary configuration is a "cross-point" memory array, which comprises a first set of parallel conductive lines covered by an insulating layer, over which lies a second set of parallel conductive lines, perpendicular to the first lines. One set of conductive lines is referred to as the "bit" lines, and the other set of conductive lines is referred to as the "word" lines. The magnetic memory cells can be sandwiched between the bit lines and the word lines at their intersections.

Summary of the Invention

[0007] In one embodiment of the present invention, a method of forming a magnetic memory cell comprises providing a first conductive layer as a blanket layer, providing a barrier layer as a blanket layer over the first conductive layer, and providing a second conductive layer as a blanket layer over the barrier layer. The method further comprises providing a hard mask over the second conductive layer, wherein the hard mask defines the region in which the magnetic memory cell is formed, etching the second conductive layer to form an upper portion of the magnetic memory cell, and forming a spacer around the upper portion of the magnetic memory cell. The method further comprises etching the barrier layer and the first conductive layer to form a lower portion of the magnetic memory cell, wherein conductive particles of the first conductive layer may be thrown up along a sidewall of the magnetic memory cell as byproducts of the etching of the first conductive layer, and oxidizing the magnetic memory cell, thereby transforming the conductive particles into nonconductive particles.

[0008] In another embodiment, a method of forming a magnetic memory cell comprises providing a first conductive layer, a barrier layer, and a second conductive layer as blanket layers, providing a hard mask over the second conductive layer, wherein the hard mask defines the region in which the magnetic memory cell is formed, and etching the second conductive layer and the barrier layer to form an upper portion of the magnetic memory cell. The method further comprises partially oxidizing the first conductive layer such that at least a portion of the first conductive layer is transformed into an insulating material, at least partially etching the portion of the first conductive layer that was transformed into an insulating material during the partial oxidizing step, and repeating the partial oxidizing and partial etching steps until the first conductive layer forms a lower portion of the magnetic memory cell.

[0009] In another embodiment, a magnetic memory cell comprises a lower layer comprising a first conductive material, a middle layer comprising an insulating material, and an upper layer comprising a second conductive material. The magnetic memory cell further comprises a nonconductive layer comprising an oxide of the first conductive material, wherein the nonconductive layer is coated along a sidewall of the magnetic memory cell such that it can be in contact with both the upper and lower layers.

[0010] In another embodiment, a magnetic memory cell comprises a lower layer comprising a first conductive material and a middle layer comprising an insulating material. The magnetic memory cell further comprises an upper layer comprising a second conductive material surrounded by a spacer material and at least one sidewall coated with oxidized particles of the first conductive material.

Brief Description of the Drawings

[0011] These and other features and advantages of the invention will now be described with reference to the drawings of certain preferred embodiments, which are intended to illustrate, and not to limit, the invention. In the figures, like reference numerals are used to refer to like elements.

[0012] Figure 1 illustrates a plurality of conventional TMR magnetic memory cells.

[0013] Figure 2 illustrates a plurality of magnetic memory cells with insulating spacers adjacent to the sense layers.

[0014] Figures 3A-3G illustrate the formation of a magnetic memory cell in accordance with one embodiment of the invention.

[0015] Figures 4A-4E illustrate the formation of a magnetic memory cell in accordance with another embodiment of the invention.

Detailed Description of the Preferred Embodiments

[0016] For purposes of illustration, various embodiments of the invention will be described in the context of a TMR magnetic memory cell having a particular configuration. The details associated with this specific configuration are set forth to illustrate, and not to limit, the invention. For example, the invention can be implemented with TMR magnetic memory cells having alternative configurations or with other types of memory cells. The scope of the invention is defined only by the appended claims.

[0017] Figure 1 illustrates a plurality of conventional magnetic memory cells 10 formed on a metal conducting line 12, preferably copper or aluminum, which is deposited on a substrate (not shown). The conducting line 12 extends to the right and to the left of the page. The memory cells 10 can be formed by first depositing a pinned layer 14 on the conducting line 12, depositing an insulating barrier layer 16 over the pinned layer 14, and depositing a sense layer 18 over the barrier layer 16. The pinned layer 14, barrier layer 16, and sense layer 18 can then be patterned and etched to form the memory cells 10 using methods that are well-known to those of skill in the art.

[0018] The pinned layer 14 may comprise a stack of magnetic and associated adjacent sublayers. For example, the pinned layer 14 may comprise a tantalum seed sublayer, a nickel-iron seed sublayer, a magnesium oxide, irridium-manganese, platinum-manganese or nickel-manganese pinning sublayer, and a nickel-iron, nickel-iron-cobalt, cobalt-iron or nickel-iron-chromium sublayer. The barrier layer 16 is preferably thin enough to allow the tunneling of electrons from the sense layer 18 to the pinned layer 14. The barrier layer 16 may comprise, for example, aluminum oxide, having a thickness within the range of about 0.5 nm to about 3 nm, preferably within the range of about 1 nm to about 2 nm. Like the pinned layer 14, the sense layer 18 may comprise a stack of magnetic and associated adjacent blanket sublayers. For example, the sense layer 18 may comprise a tantalum sublayer, a tungsten nitride sublayer, and a nickel-iron, nickel-iron-cobalt, cobalt-iron, cobalt or copper sublayer.

[0019] During the fabrication of a conventional magnetic memory cell 10, it is common for a thin coating of conductive material 20 to form along the sidewalls of the memory cell 10, as illustrated in Figure 1. This coating of conductive material 20 may comprise, for example, particles of the pinned layer 14 that are thrown up along the sidewalls of the memory cell 10 during the process of etching through the pinned layer 14, particularly if an etching process with a physical component is used, such as an ion milling process or a reactive ion etch.

[0020] The thin coating of conductive material 20 along the sidewalls of the memory cell 10 is undesirable because it can create a conductive path between the pinned layer 14 and the sense layer 18. Such a conductive path creates an electrical short across the barrier layer 16 that can prevent the memory cell 10 from functioning properly. Therefore, the coating of conductive material 20 along the sidewalls of the memory cells 10 can undesirably reduce the yield of the manufacturing process. Although an additional cleaning step can be performed to remove the coating of conductive material 20 from the sidewalls of the memory cells 10, such an additional step can add cost to the manufacturing process and can also have a harmful effect on the remaining structures.

[0021] Figure 2 illustrates a plurality of magnetic memory cells 10 with spacers 22 adjacent to the sense layers 18. The spacers 22 preferably comprise a nonconductive material, such as, for example, silicon nitride, diamond-like carbon, silicon carbide, or an oxide such as silicon oxide or aluminum oxide. The spacers 22 can be formed using a variety of well-known techniques. For example, the sense layer 18 can be patterned and etched with a hard or resist mask in place, followed by the deposition of a blanket layer of nonconductive material. The resulting structure can then be subjected to a spacer etch, followed by etching through the underlying pinned layer 14.

[0022] Although a coating of conductive material 20 can form along the sidewalls of the memory cells 10, the spacers 22 advantageously reduce the likelihood that such a coating will form a conductive path between the sense layer 18 and the pinned layer 14 of a given memory cell 10 by largely protecting the sense layer 18 during etching of the pinned layers 14. Therefore, the spacers 22 can advantageously reduce the number of memory cells 10 that short out, thereby increasing the yield of the manufacturing process. Even in a memory cell 10 having a spacer 22 adjacent to the sense layer 18, however, an electrical short across the barrier layer 16 can still occur due to, *inter alia*, a small point of contact 24 between the coating of conductive material 20 and the sense layer 18.

[0023] Figures 3A-3G illustrate a process for forming a magnetic memory cell 10 in accordance with one embodiment of the invention. Although the memory cell 10 of the illustrated embodiment comprises a TMR magnetic memory cell having a particular configuration, the memory cell 10 could have a wide variety of alternative configurations. For example, in the illustrated embodiment, the pinned layer 14 is the bottom layer of the memory cell 10. In other embodiments, the pinned layer 14 may be the top layer of the memory cell 10. These and many other variations will become apparent to those of skill in the art in view of the present disclosure.

[0024] The process of the illustrated embodiment begins by depositing a pinned layer 14, a barrier layer 16, and a sense layer 18 on a conductive line 12. As discussed above, the pinned layer 14 may comprise a stack of magnetic and associated adjacent sublayers, the barrier layer 16 preferably comprises a nonconductive material through which electron tunneling can occur, and the sense layer 18 may comprise a stack of magnetic and associated adjacent sublayers.

[0025] These layers can be formed using a wide variety of well-known methods and materials. For example, in some embodiments, both the pinned layer 14 and the sense layer 18 comprise a ferromagnetic material that is an alloy of any of several metals, such as, for example, iron, nickel, and/or cobalt having a thickness preferably within the range of about 1 nm to about 30 nm, more preferably within the range of about 2.5 nm to about 20 nm, and still more preferably within the range of about 5 nm to about 10 nm. In some embodiments, the barrier layer 16 comprises an oxide of a metal, such as, for example, aluminum oxide, having a thickness preferably within the range of about 0.5 nm to about 3 nm, more preferably within the range of about 1 nm to about 2 nm. Those of ordinary skill in the art will understand that these materials and thickness ranges are exemplary, and that different materials having different thicknesses could be used.

[0026] As illustrated in Figure 3A, a hard mask 30 can be deposited as a blanket layer over the sense layer 18, and then patterned and etched using a variety of conventional materials and methods. For example, the hard mask 30 may comprise Si_3N_4, SiO_3N_4, SiC, or any other suitable hard mask material, having a thickness preferably within the range of about 100 Å to about 5000 Å, more preferably within the range of about 500 Å to about 2000 Å. The hard mask 30 can be patterned using a number of well-known techniques, such as, for example, conventional photolithography and etching processes.

[0027] As illustrated in Figure 3B, the sense layer 18 is etched in the areas that are not covered by the hard mask 30. This etch can be performed using a variety of well-known processes, such as, for example, ion milling, reactive ion etching, or chemical etching. If a process involving a chemical etchant is selected, any of a number of well-known etchants can be used, such as, for example, CO_2-NH_3 or CO-NH_3. The etching of the sense layer 18 preferably stops at the barrier layer 16. The hard mask 30 is also partially etched during the etching of the sense layer 18.

[0028] After the sense layer 18 is etched, the resulting structure can be optionally oxidized to transform the outer portions of the sense layer 18 into a nonconductive material (not shown). This optional oxidation step can be performed using an oxidant such as, for example, O_3, at a flow rate preferably within the range of about 1 sccm to about 1000 sccm, more preferably within the range of about 100 sccm to about 500 sccm. In other embodiments, this optional oxidation step involves using O_2 as an oxidant during a plasma oxidation process. Because this optional oxidation step reduces the amount of conductive surface area around the sides of the sense layer 18, it advantageously reduces the likelihood of a conductive path forming between the pinned layer 14 and the sense layer 18.

[0029] As illustrated in Figure 3C, a blanket layer of spacer material 22 is deposited over the existing layers. The spacer material 22 can be any suitable material (e.g., Si_3N_4) but preferably comprises a low k electrical insulator, with k value preferably less than 3.5, more preferably less than 3.0. A variety of materials exist that can be used as the spacer material 22, such as, for example, silicon nitride, diamond-like carbon, silicon carbide, or an oxide such as silicon oxide or aluminum oxide.

[0030] The spacer material 22 can be deposited using any suitable process, such as, for example, physical vapor deposition or chemical vapor deposition. In some embodiments, the thickness of the layer of spacer material 22 preferably falls within the range of about 5 nm to about 100 nm, and more preferably within the range of about 20 nm to about 40 nm.

[0031] As illustrated in Figure 3D, the layer of spacer material 22 is etched, preferably using an anisotropic etch process that preferentially etches the horizontal portions of the layer of spacer material 22 relative to the vertical portions of the layer of spacer material 22. Therefore, an etching process with a physical component is preferably used, such as an ion milling process or a reactive ion etch. In some embodiments, for example, a reactive ion etch is used with an appropriate etchant for the selected spacer material 22. For example, in some embodiments, the spacer material 22 comprises silicon nitride and the etchant comprises CF_4 or CHF_3. In other exemplary embodiments, the spacer material 22 comprises diamond-like carbon and the etchant comprises oxygen-based plasma. In other exemplary embodiments, the spacer material 22 comprises silicon carbide and the etchant comprises CF_4, CH_2F_2, or C_2F_6.

[0032] In the embodiment illustrated in Figure 3D, the spacer etch process stops at the barrier layer 16. In other embodiments, the spacer etch process continues until the pinned layer 14 is reached. In these embodiments, the barrier layer 16 is also etched as part of the same process that etches the layer of spacer material 22.

[0033] As illustrated in Figure 3E, after the spacer etch process is complete, the remaining layers are etched. In some embodiments, the process used to etch the remaining layers is substantially similar to the process used to etch the sense layer 18. This process may comprise, for example, ion milling, reactive ion etching, or chemical etching, and may use an etchant such as, for example, CO_2-NH_3 or CO-NH_3. The hard mask 30 is also partially etched during the etching of the pinned layer 14.

[0034] As the pinned layer 14 is etched, a thin coating of conductive material 20 may form along the sidewalls of the memory cell 10. The thin coating of conductive material 20 may comprise particles of the pinned layer 14 that are thrown up as byproducts of the etching process of the pinned layer 14. As discussed above, the thin coating of conductive material 20 may form a conductive path between the pinned layer 14 and the sense layer 18, thereby creating an electrical short across the barrier layer 16 that can cause the memory cell 10 to malfunction. Although the spacers 22 minimize the amount of exposed conductive surface area around the sides of the sense layer 18, and thus reduce the likelihood of a conductive path forming between the pinned layer 14 and the sense layer 18, such a conductive path can still exist if there is even only a small point of contact 24 between the thin coating of conductive material 20 and the sense layer 18.

[0035] Accordingly, to further reduce the likelihood of a conductive path forming between the pinned layer 14 and the sense layer 18, the thin coating of conductive material 20 can be oxidized to transform the conductive material 20 into a nonconductive material 36, as illustrated in Figure 3F. This oxidation step can be performed using an oxidant such as, for example, O_3, at a flow rate preferably within the range of about 1 sccm to about 1000 sccm, more preferably within the range of about 100 sccm to about 500 sccm. In other embodiments, this oxidation step involves using O_2 as an oxidant during a plasma oxidation process. It should be understood that, although the thin coating of nonconductive material 36 is illustrated as one continuous layer in Figures 3E-3F, it may be formed as a discontinuous layer.

[0036] As illustrated in Figure 3G, the remaining portion of the hard mask 30 is removed to complete the process of forming the memory cell 10. By oxidizing the conductive material 20, thereby transforming it into a nonconductive material 36, the likelihood of a conductive path forming between the pinned layer 14 and the sense layer 18 due to a small point of contact 24 between the layer of nonconductive material 36 and the sense layer 18 is substantially reduced. Accordingly, the number of memory cells 10 within an MRAM array that malfunction due to electrical shorts is reduced, and the yield of the manufacturing process for the MRAM device is advantageously improved.

[0037] Figures 4A-4G illustrate an alternative process for forming a magnetic memory cell 10 in accordance with one embodiment of the invention, which is somewhat similar to the embodiment of the invention described above. For example, as illustrated in Figures 4A-4B, the process begins with the same steps described above in connection with Figures 3A-3B.

[0038] In the present embodiment, however, after the sense layer 18 is etched, the resulting structure is repeatedly subjected to alternating partial oxidation and partial etch steps until the memory cell 10 is formed. In some embodiments, the partial oxidation steps are performed by subjecting the structure to plasma oxidation using a process that is substantially similar to the optional oxidation step described above in connection with Figure 3B. As illustrated in Figure 4C, when the structure is subjected to plasma oxidation, the outer or sidewall portions 40 of the sense layer 18 and the upper portion 42 of the pinned layer 14 are transformed into a nonconductive material, except for the portions that are protected under the hard mask 30.

[0039] As illustrated in Figure 4D, the pinned layer 14 can then be partially etched because, even if particles from the upper portion of the pinned layer 14 are deposited along the sidewalls of the structure as byproducts of the etching process, the particles are nonconductive and thus unlikely to cause an electrical short across the barrier layer 16. In addition, the grown sidewall spacer in the form of outer portions 40 further reduces the likelihood of a short forming across the barrier layer 16. To perform the partial etch of the pinned layer 14, an etching process with a physical component is preferably used, such as an ion milling process or a reactive ion etch. The partial etch preferably stops before the portion of the pinned layer 14 below the upper portion 42 is reached, such that only nonconductive particles tend to be thrown up along the sidewalls of the memory cell 10 as byproducts of the etching process.

[0040] The steps illustrated in Figures 4C-4D can be repeated cyclically until the entire pinned layer 14 has been oxidized and etched. In a preferred embodiment, both the oxidation and the etching steps can be performed in situ within the same tool. Then, as illustrated in Figure 4E, the remaining portion of the hard mask 30 can be removed to complete the process of forming the memory cell 10. By repeatedly partially oxidizing and etching the pinned layer 14 such that only nonconductive particles can be deposited along the sidewalls of the memory cell 10 during the fabrication process, the likelihood of a conductive path forming between the pinned layer 14 and the sense layer 18 is substantially reduced. Accordingly, the number of memory cells 10 within an MRAM array that malfunction due to electrical shorts is reduced, and the yield of the manufacturing process for the MRAM device is advantageously improved.

[0041] In addition, the process illustrated in Figures 4A-4E is advantageously self-aligning because the region under the hard mask 30 is protected from both oxidation and etching. Therefore, although the process involves repeating a series of alternating oxidation and etching steps, the process involves only a single masking step. Because no additional masks are needed to perform the alternating oxidation and etching steps, the process can advantageously be performed at a relatively low cost.

[0042] Although this invention has been described in terms of certain preferred embodiments, other embodiments that are apparent to those of ordinary skill in the art, including embodiments that do not provide all of the features and advantages set forth herein, are also within the scope of this invention. Accordingly, the scope of the present invention is defined only by reference to the appended claims.